Analysis of Different Bus Structures for Transport Triggered Architecture

Raimo Mäkelä, Jarmo Takala and Olli Vainio

Tampere University of Technology, Institute Of Digital and Computers Systems
P.O. Box 553
FIN-33101 Tampere, Finland
ragimund@cs.tut.fi, jarmo.takala@tut.fi, and olli.vainio@tut.fi

Abstract

In computer system design, speed and power dissipation estimates are needed as early as possible in the design flow. This is particularly important for critical subsystems, such as the bus structures. This paper compares the delay and power consumption of bus structures for the Transport Triggered Architecture. A synthesis based standard cell design approach is assumed. The comparisons are done with models which use data from the standard cell libraries. The models are evaluated by comparing them to the timing information and the power analysis results from the synthesis tools.

1. Introduction

Power consumption is one of the most important design parameters in VLSI design. However, the VLSI designer has to take care of the delay of the system, which is usually the most important design parameter. This comes from the fact that portable devices should have as long battery life as possible and at same time there are demands for increased functionality and especially computation power. Therefore, power consumption is a parameter which is tried to be minimized but delay is a hard-constraint for VLSI designer.

In general, designs need to be tailored according to the application for minimizing the power consumption. In order to alleviate such tailoring effort, tools-assisted design methodologies should be used. Such a design methodology for application-specific programmable processors is the MOVE framework [1], which allows semi-automatic design space exploration. The methodology is based on Transport Triggered Architectures (TTA) [2], which is a processor template supporting instruction level parallelism where heterogeneous function units can be included along the internal multi-port busses. In principle, TTAs remind VLIW machines. The TTA is extremely modular and, therefore, it is a good basis for designing application-specific processors.

The MOVE design tools include a processor generator, which creates automatically VHDL description of the final processor architecture. While VHDL is a standard language for designing complex systems, it has limitations with standard cell technologies. For example, the MOVE design tools assume that the bus structures are realized with the aid of tri-state buffers, which are poorly supported by the commercial logic synthesis tools. This is mainly due to timing difficulties with the enable signals of tri-state buffers in synthesis. Therefore, different bus structures should be used in this framework.

In order to compare different bus structures, the characteristics cannot be obtained with the aid of logic synthesis. The original bus structure described in VHDL may be lost during the logic optimization when the commercial synthesis tools are used to obtain data for a comparison. The structure can be kept by using well defined bus models in comparison.

In this paper, AND/OR, multiplexer, and segmented multiplexer bus structures are selected as possible bus structures, which can be implemented with standard cells for TTA. These structures and the tri-state bus are compared in order to find the best bus structure for the TTA. The comparisons are done with models which give the worst case delay and power approximation for each bus structure. The models are based on the skeletal structures where all structural choices, for example for multi input gates, are selected in the worst case manner. Well known equations and data from the standard cell library, provided by the process manufacturer, are used to get reliable models for the structures. Moreover, the calculated results are compared to the timing information and the power analysis results from the synthesis tools.

The content of the paper is as follows. The modeling principles and the assumptions used in the equations are explained in Chapter 2. The bus architectures are introduced in Chapter 3 and the results are given in Chapter 4. The paper is concluded in Chapter 5.

2. Modeling Principles

This chapter introduces the equations used as the basis in modeling the bus structures to be compared. The bus structures can be implemented using standard cells and it is reasonable to use the data from actual standard cell libraries in calculations.

2.1 Wire Models

Wires are modeled with the lumped RC model [3]. The resistance (R_{uw}) and capacitance (C_{uw}) of a unit wire are the product of resistance (R_{ul}) and capacitance (C_{ul}) per unit length, respectively, and the length of unit wire (L_{uw}). Resistances and capacitances are taken from the wire model in the standard cell library. The variable 'slope' from a standard cell library can be used for L_{uw}.

The resistance and capacitance for nodes in a circuit are defined as:

$$R_w = NR_{uw} \quad (2.1)$$

$$C_w = NC_{uw} \quad (2.2)$$

where N is the fanout, i.e., the number of inputs connected to the driving output.

2.2 Delay Estimation

The delay estimation is done with a linear delay model. In the model, the delay of a circuit is the sum of four parts: Slope delay (D_S), intrinsic delay (D_I), transition time (D_T), and connect delay (D_C). [3] [4]

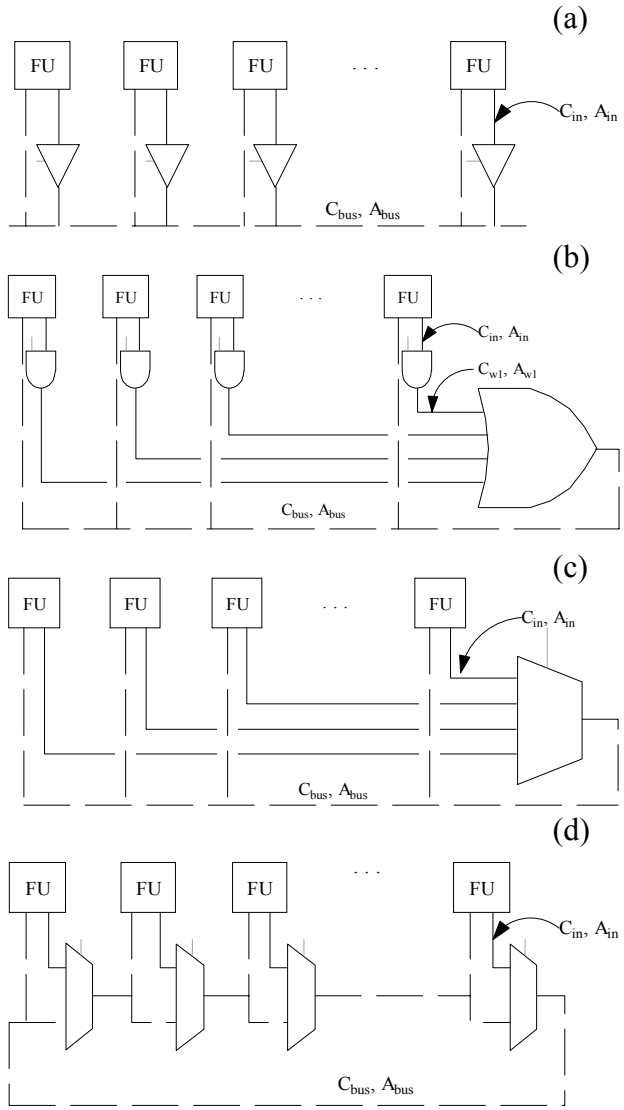

Figure 1. The compared bus structures. Parts indexed as bus are drawn with a dashed line.

The slope delay is the part of the gate delay caused by the input transition time. It can be calculated from the transition time of the previous gate as follows.

$$D_S = S \cdot D_{Tprevious} \tag{2.3}$$

The scaling factor S is obtained from the standard cell library.

The intrinsic delay is the part of gate delay that is independent of the usage of gates. This is a fixed delay of a gate, also called the zero load delay of a gate.

The transition time is a delay caused by the capacitive load in the output of a gate. The transition time can be calculated as:

$$D_T = R_{drive}\left(C_w + \sum_g C_g\right) \tag{2.4}$$

where R_{drive} is the output resistance of gate and the C_g is the capacitance of the input connected to this output.

The connect delay is the time taken by the change in voltage to arrive through the wire from the output of the gate to the input of another gate. The worst case of the connect delay can be calculated from the R_w, C_w, and C_g as follows.

$$D_C = R_w\left(C_w + \sum_g C_g\right) \tag{2.5}$$

2.3 Power Estimation

The power consumption in CMOS circuits is divided to two components: dynamic and static (P_S) power consumption. Further, the dynamic power consumption is divided to switching (P_D), and internal (P_I) power consumption. [5]

The switching power consumption is caused by the charging and discharging of capacitive loads caused by the wires and the fanout gate inputs connected to the outputs of gates. The switching power consumption in a circuit can be calculated by using (2.6). V_{DD} is the supply voltage and C_z is the capacitive load connected to output Z where the transition probability is A_z at the frequency f. The part of C_z caused by wires is a function of fan out; which means that there is one unit wire per each input connected to the output.

$$P_D = \frac{1}{2}V_{DD}^2 f \sum_z (C_z A_z) \tag{2.6}$$

The internal power consumption is the power consumption inside a gate. It includes both the switching and the short circuit [5] power consumption in the gate. The internal power consumption can be calculated by using (2.7). Internal energy for output Z (E_z) is given by the process manufacturer as the function of the transition time in the input of the gate, see (2.8), where E_{int} is the constant part of the energy.

$$P_I = f \sum_z (E_z A_z) \tag{2.7}$$

$$E_z = E_{\text{int}} + E(D_{Tprevious}) \tag{2.8}$$

The static power consumption is consumed all the time in circuits, even when transistors block any path from the power supply to the ground. The data is obtained from the standard cell libraries.

3. Bus Structures

In this paper four different bus structures are modeled and compared: A tri-state bus (a), a multiplexer bus (b), an AND/OR bus (c), and a segmented multiplexer bus (d). The structure of each bus is illustrated in Figure 1.

There are several parameters, which are common to all bus structures: The number of inputs (N_{in}) and outputs (N_{out}) to the bus, activities on the bus (A_{bus}) and at the input of the bus (A_{in}), and capacitances in the bus (C_{bus}) and in the input (C_{in}). The capacitances are not the same for every bus structure and they are defined later through their wire and input components.

3.1 Tri-state Bus

The sizing of tri-state buffers affects strongly the delay of this structure. When the size of a tri-state buffer increases, its output resistance decreases and the input and output capacitances, as well as internal energy, increases. In this paper, the sizing is modeled with a linear model by fitting a line to data in the standard cell library. The size of the tri-state buffer is adjusted in such a manner that the delay is kept near the delay of the AND/OR bus structure.

The wire and input capacitances of the tri-state bus are given by (3.1) and (3.2), respectively.

$$C_{busw} = C_{uw}(N_{out} + N_{in}), \quad C_{inw} = C_{uw} \tag{3.1}$$

$$C_{busg} = N_{in}C_{buf\_out} + N_{out}C_{load}, \quad C_{ing} = C_{buf\_in} \tag{3.2}$$

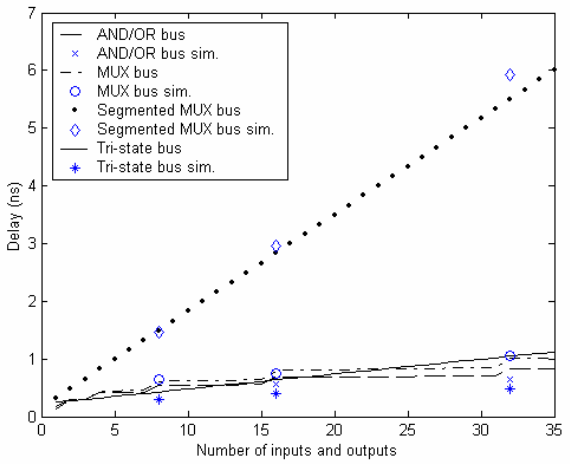

Figure 2. The comparison of the delay models to the timing information from the synthesis tools.

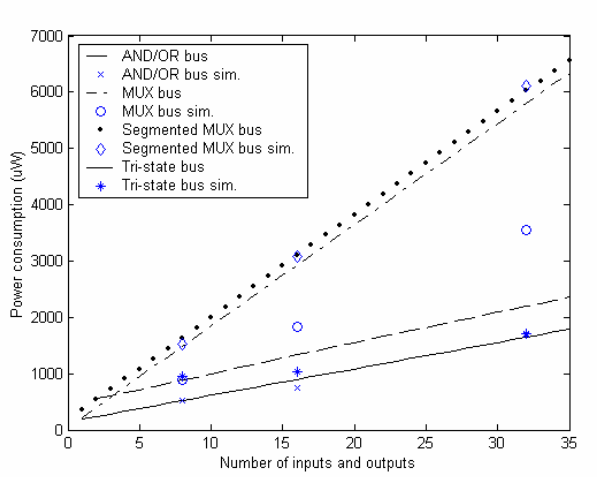

Figure 3. Comparison to the power analysis result from the synthesis tools.

3.2 AND/OR Bus

A tree of two-input OR gates is used to model the multi-input OR gate in the AND/OR bus structure. The average activity at the input of the OR gate (A_{wl}) is equal to A_{bus}/N_{in}, based on the functioning of the AND/OR bus. Therefore, activity inside the OR gate varies, which is estimated by average activity (A_{avg}), see (3.3).

$$A_{avg} = \frac{(N_{in} - 2)}{N_{in} \cdot \log_2(N_{in}/2)} A_{bus} \qquad (3.3)$$

The wire and input capacitances of the AND/OR bus are given by (3.4) and (3.5), respectively.

$$C_{busw} = C_{uw} N_{out}, \quad C_{wl} = C_{inw} = C_{uw} \qquad (3.4)$$

$$C_{busg} = N_{out} C_{load}, \quad C_{ing} = C_{and\_in} \qquad (3.5)$$

3.3 Multiplexer Bus

Activity at the input goes inside the multi-input multiplexer in the multiplexer bus. The multiplexer is modeled similarly to the OR gate in the AND/OR bus, with the tree structure. A difference is that the input activity affects the activity of nodes inside the multiplexer. So, when $A_{in}=A_{bus}$ the activity in the nodes is also A_{bus} and when $A_{in}=A_{bus}/N_{in}$, A_{avg} can be used for the activity in the nodes.

The wire and input capacitances of the multiplexer bus are given by (3.6) and (3.7), respectively.

$$C_{busw} = C_{uw} N_{out}, \quad C_{inw} = C_{uw} \qquad (3.6)$$

$$C_{busg} = C_{load} N_{out}, \quad C_{ing} = C_{mux\_in} \qquad (3.7)$$

3.4 Segmented Multiplexer BUS

In the segmented multiplexer bus, multiplexers divide the bus wire into several segments. The wire and input capacitances of the segmented multiplexer bus are given by (3.8) and (3.9), respectively.

$$C_{busw} = C_{uw}(N_{out} + N_{in}), \quad C_{inw} = C_{uw} \qquad (3.8)$$

$$C_{busg} = C_{mux\_in} N_{in} + C_{load} N_{in}, \quad C_{ing} = C_{mux\_in} \qquad (3.9)$$

4. Results

The final equations have been derived for the bus structures using the theory and assumptions introduced above. The results are calculated using Matlab [6].

The delay and power models are compared to the timing information and the power analysis results, respectively, from the actual synthesis tool. The results are gathered to Figures 2 and 3. Calculations have been done for a 0.16 micron technology with 1.6 V supply voltage. The clock frequency is 50MHz and the bus width is 32 bits.

The delay and power consumption of the four structures are compared in Figures 4 to 7 for the case $N_{in}=N_{out}$. The tri-state bus is the most sensitive to changes in wire length, see Figure 4. In the results shown in the figure, wire length model is changed from constant to variable wire length model and increment in delay is plotted as a function of N_{in} and N_{out}. In the constant wire length model, L_{uw} is kept in minimum value for all values of N_{in} and N_{out}. In the variable wire length model, L_{uw} increases when N_{in} or the N_{out} increases. The variable wire length model is used in later calculations. The segmented multiplexer bus has the largest delay, see Figure 5. For the purpose of clarity, the delay is normalized by the maximum value.

The change in input activity affects mostly the power consumption of the multiplexer bus (see Figure 6). In these calculations A_{in} is changed from A_{bus}/N_{in} to A_{bus} and the increment in the power consumption is plotted as function of N_{in} and N_{out}.

The normalized power consumption of different bus structures is plotted in Figure 7. The input activity $A_{in}=A_{bus}$ is used in the calculations. The segmented multiplexer bus and the multiplexer bus have the highest power consumption. The power consumption of the tri-state bus increases rapidly when the number of inputs and outputs increases.

The power consumption of AND/OR is uniformly effected by both N_{in} and N_{out}. Whereas the power consumption of the both busses based on multiplexers are more dependent on N_{in} than N_{out}. The power consumption of the tri-state bus increases most on the diagonal of the data matrix.

5. Conclusions

The following conclusions are based on comprehensive comparisons for different values of N_{in} and N_{out}, which cannot be graphically illustrated due to lack of space.

The result of the comparison to the data from the actual synthesis tool was as expected. Only in the case of the tri-state bus the delay calculated with models is too much overestimated and the power consumption is under estimated especially for smaller busses. From more detailed results from the actual

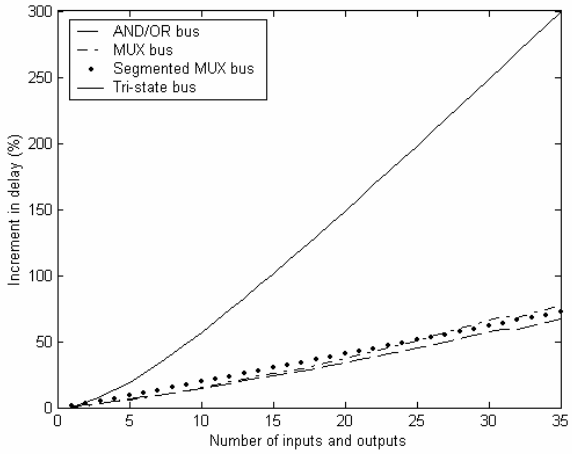

Figure 4. Increase in delay as function of N_{in}=N_{out}.

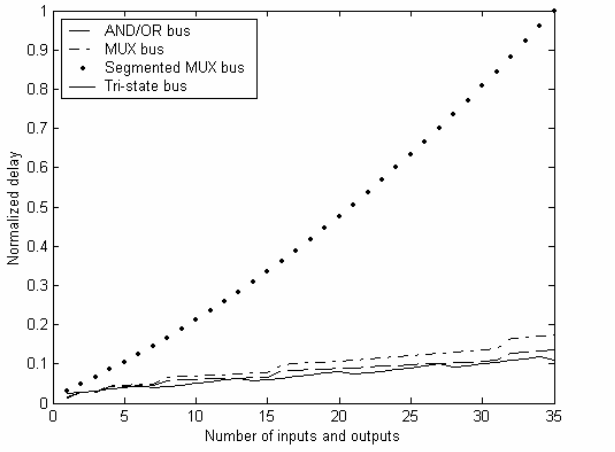

Figure 5. Normalized delay as function of N_{in}=N_{out}.

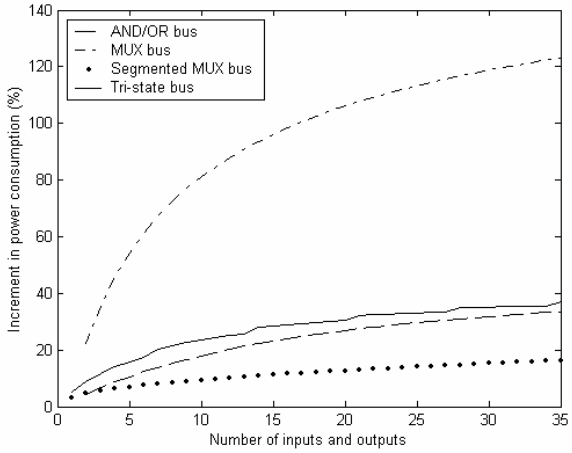

Figure 6. Increase in power as function of N_{in}=N_{out}.

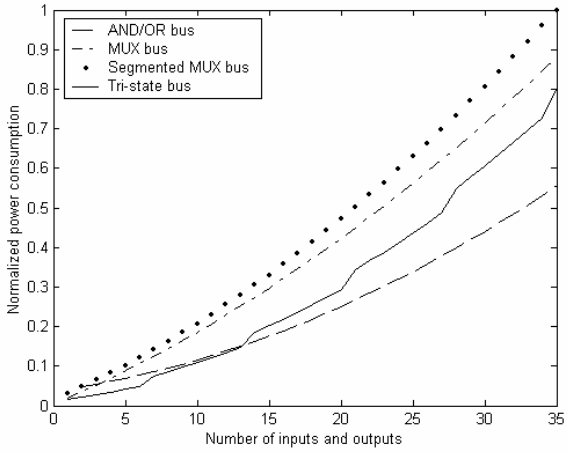

Figure 7. The power consumption of bus structures.

synthesis tool it can be seen that net switching power for each tri-state buffer almost halves when the number of tri-state buffers in the bus doubles. Logically switching power should be almost the same for each tri-state buffer with any number of tri-state buffers connected to the bus, if the buffer size is kept the same. This leads to the conclusion that the actual synthesis tool does not extract right switching activities for nets in the tri-state bus if only the switching activities of the inputs are known.

From the results it can be seen that the equations highlight well the characteristics for every bus structure. The tri-state bus has large capacitances on the bus driven by a single buffer, which is why it is the most sensitive to increments in the wire length. The segmented multiplexer bus has the highest delay because of cascaded multiplexers. The highest sensitivity to input activity can be explained by the increasing activity inside a large multiplexer when the input activity increases. High power consumption in the multiplexer bus and the segmented multiplexer bus is caused by the large capacitance in highly active nodes. In the tri-state buffer case, the capacitance on the bus node increases rapidly.

The AND/OR bus seems to be strong in every area. It is fast, it has low power consumption, and it has high immunity to changes in parameters. Segmented multiplexer bus is slow when used as ordinary bus but its strength may be in multiple data transmission in parallel by one bus.

6. References

[1] H. Corporaal, M. Arnold. 1998. “Using transport triggered architectures for embedded processor design” *Integrated Computer-Aided Engineering*, vol. 5, no. 1, pp. 19-38.

[2] H. Corporaal. 1998. *Microprocessor Architecture: From VLIW to TTA*. John Wiley & Sons. 407 p.

[3] J.M.. Rabaey. 1996. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall International, Inc. 702 p.

[4] N.H.W.Weste. Kamran Eshraghian. 1994. *Principles of CMOS VLSI Design: A System Perspective*. Second Edition. Addison-Wesley. 713 p.

[5] A. Bellaouar, M.I. Elmastry. 1995. *Low-Power Digital VLSI Design: Circuits and Systems*. Kluwer Academic Publishers. 530 p.

[6] http://www.mathworks.com